ARRAY ARCHITECTURE AND OPERATING METHODS FOR DIGITAL MULTILEVEL NONVOLATILE MEMORY INTEGRATED CIRCUIT SYSTEM

ABSTRACT OF THE DISCLOSURE

Memory array architectures and operating methods suitable for super high density in the giga bits for multilevel nonvolatile memory integrated circuit system. The array architectures and operating methods include: (1) an Inhibit and Select Segmentation Scheme; (2) a Multilevel Memory Decoding Scheme that includes a Power Supply Decoded Decoding Scheme, a Feedthrough-to-Memory Decoding Scheme, a Feedthrough-to-Driver Decoding Scheme, and a Winner-Take-All Kelvin Memory Decoding Scheme; (3) a constant-total-current-program scheme; (4) includes fast-slow and 2-step ramp rate control programming; and a reference system method and apparatus, which includes a Positional Linear Reference System, a Positional Geometric Reference System, and a Geometric Compensation Reference System. The apparatus and method enable multilevel programming, reading, and margining.